Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.051”**

**.058”**

**DIE ID**

**1**

**8**

**5**

**C**

**V-**

**V+**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V- (Back may be left floating)**

**Mask Ref: 185C**

**APPROVED BY: DK DIE SIZE .051” X .058” DATE: 3/13/17**

**MFG: NATIONAL SEMI THICKNESS .014” P/N: LM285-1.2**

**DG 10.1.2**

#### Rev B, 7/19/02